

9.3.5 IC7520 control (see Fig. 9.4 and Fig. 9.3)

The error amplifier (block A in Fig. 9.4) compares the feedback voltage Vpin 14 with an internal reference voltage of 2V5. The output voltage Verror-out of this error amplifier is fed to another comparator (block B in Fig. 9.4). This comparator compares the Verror-out and the current sense voltage Vpin 7. As soon as the current sense voltage Vpin 7 becomes higher than the output -voltage of the error amplifier Verror-out, the comparator B gives a spike (the output of comparator B is the so called current sensing output-voltage Vcs out).

9.3.6 Flip flop

Flip flop (block C in Fig. 9.4) drives the output pin 3 (Vpin 3) via a buffer amplifier (block D). The flip flop is set by positive edge of the output of the oscillator (V osc) and reset by the spike Vcs out. As a result the pulse Vpin 3 becomes "high" (T-on starts) by the positive edge of Vosc from the internal oscillator and "low" (T-on stops) by the spike of Vcs out (the T-on start will be delayed in case the transformer is not yet demagnetised; see the slow-start procedures).

9.3.7 Stable load and increasing / decreasing load (see Fig. 9.3)

In case of a stable load, the feedback voltage Vpin 14 (and so also the maximum current sense voltage Vpin 7) remains the same. As a result the T-on and so the duty cycle will remain the same.

In case of an increasing load, the secondary output voltage decreases. The voltage on pin 14 would like to decrease which causes Verror-out to increase. As a result comparator B will give the pulse later; Vpin 3 will be "high" for a longer period (longer T-on so the duty cycle increase) and so the secondary output voltages will be increased (corrected). This will give a new balance of feedback voltage Vpin 14 and the internal 2V5 reference voltage, at a new larger duty cycle. As a result of the longer T-on, the maximum I-prim increases, so more energy can be stored in the transformer. In this way more energy will be supplied to the load.

In case of a decreasing load, the secondary output voltage increases. The voltage on pin 14 would like to increase which causes Verror-out to decrease. As a result comparator B will give the pulse earlier, Vpin 3 will be "high" for a shorter period (shorter T-on so the duty cycle decrease) and so the secondary output voltages will be decreased (corrected). This will give a new balance off feedback voltage Vpin 14 and the internal 2V5 reference voltage, at a new smaller duty cycle.

As a result of the shorter T-on, the maximum I-prim decreases, so less energy can be stored in the transformer. In this way less energy will be supplied to the load.

In case the demagnetisation of the transformer is not finished, the positive edge from the oscillator, which will start a new cycle, will be overruled (via buffer block D) as being the starting point of T-on. As a result the T-on will be delayed and so the frequency of the SMPS will go down. This procedure is used during start-up.

9.3.8 Peak current limiting

Peak current limiting is realised by an internal clamp at Vpin 7 at 1V DC. Via this clamp the Vpin7 can never exceed 1V DC and so the maximum value of I-prim (maximum current through FET 7518) is determined.

In case the load needs more than the maximum power, by then the I-prim is already at his maximum level so the SMPS will goin overload protection (see foldback principle explained at overload protection).

9.3.9 Cycle-by-cycle control

The T-on control is controlled on a cycle-by-cycle basis (because of the flip flop block C in IC7520). This means that in every cycle the T-on is determined again. By doing so the secondary voltages control, peak current limitation and all protections can be very accurate and fast.

9.3.10 Slow-start

As soon as Vpin 1 > 14V5 DC the SMPS will start-up. This will be done by a slow-start procedure (both the frequency and the duty cycle will be built up during slow-start). The following 3 phenomena's take place during start-up:

- The frequency will slowly increase up the nominal frequency (70 kHz for normal operation and 20 kHz for standby). This is realised via the demagnetisation function at pin 8; via this "DEMAG" function, FET 7518 will only be driven into conduction (T-on will only become "high") when T5545 is totally demagnetised.
- The voltage at pin 5 determines the foldback point. As during start-up this Vpin 5 is gradually built-up, the foldback point will also gradually increase (see foldback principle explained at overload protection).
- The duty cycle will slowly increase beginning at the absolute lowest duty cycle possible. The maximum duty cycle is determined by C2530 at pin 11 IC7520, as C2530 is unchanged at start-up, the power starts up at the lowest possible duty cycle.

9.3.11 Standby mode

In standby mode the load decreases (see description of standby on the secondary side) under a certain threshold level. The SMPS will determine this threshold level and so switch to the so called "reduced frequency mode" at 20 kHz. This minimal load threshold level is determined by R3532 at pin 12.

- 70 kHz. In normal operation mode the internal oscillator gives 70 kHz. This frequency is controlled by C2531 at pin 10 IC7520 and by R3537 pin 16 IC7520.
- 20 kHz. In standby mode the internal oscillator gives 20 kHz. This frequency is controlled by R3536 at pin 15 IC7520.

9.3.12 FET 7518 gate regulation

D6524 prevents pin 3 of IC7520 from becoming negative (this will destroy the IC) due to stray inductance in the gate part. The safety resistor R3525 limits the drive current to the gate of FET 7518.

9.3.13 Typical values

In a stable situation Vpin 14 is typical 2V5.	
Mains Voltage:	110V, 90 - 276V 220 - 240V, 150 - 276V
Mains frequency:	50 Hz / 60 Hz
Power Consumption:	
in normal mode	14": 43W +/- 10% 20": 52W +/- 10% 21": 57W +/- 10%
in stand-by mode	< 10W < 3W option

9.4 Protections

9.4.1 Over voltage protection of the secondary voltages

After start-up is the supply voltage Vpin 1 taken over by positive winding 1 - 2, and so after start up Vpin 1 is a