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Model Name : ZIVY0
File Name : LA-A921PR03
BOM P/N:4319xxxxxx -- ZIVY0

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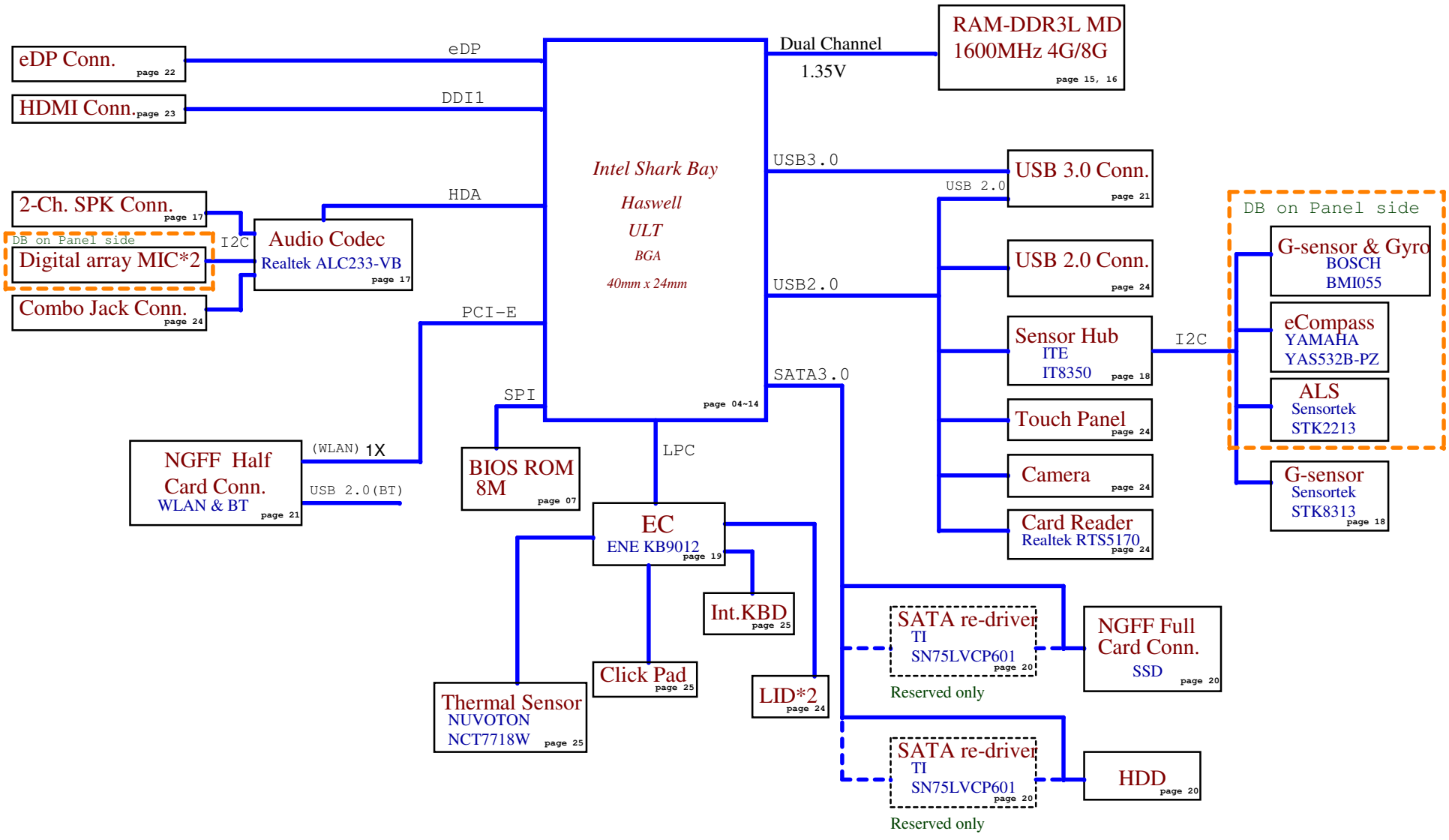
ZIVY0 M/B Schematics Document

Intel SharyBay ULT Processor

2013-12-01
REV:1.0

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Voltage Rails

power plane	B+	+5VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS
State		+3VALW		
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
76 LEVEL	X76@
Unpop	@
CPU OPTION	CPU1@ ~ CPU5@
DRAM Option	H4G@ E4G@ S4G@ M4G@ S8G@ E8G@ H8G@ H8G@
KB9012	9012@
KB9022	9022@
No Re-driver	NR@
TI Re-driver	TI@
PARADE Re-driver	8520C@
Segate HDD	HDDSG@
WD HDD	HDDWD@
EMI PART	EMI@
ESD PART	ESD@
SSD-SATA	SSDSATA@

EC SM Bus1 address

Device	Address
Smart Battery	
Charger	
Home Key Button	01100000

EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W	
SharkBay ULT SML1	1001100x

CPU SM Bus address

Device	Address
Touch Pad	

CPU SML0 Bus address

Device	Address
--------	---------

USB 2.0 Port Table

USB 2.0 Port	2 External USB Port
0	USB 2.0 Port (I/O Board)
1	USB 3.0/2.0 Port (MB)
2	
3	Card Reader
4	Touch Screen (reserve)
5	Camera
6	Mini Card (WLAN/BT)
7	Sensor Fusion

USB 3.0 Port Table

Port	
1	
2	USB 3.0 Port (MB)
3	
4	

PCIe Port Table

Port	Lane	
1		
2		
3		
4		WLAN
5	0	
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

SATA Port Table

Port	
3	NGFF SSD(SATA)
2	
1	
0	HDD

SMBUS Control Table

	HOST	Changer	BATT	KB9022	CPU	HomeKey	Touch Pad	Thermal sensor NCT7718W
EC_SMB_CK1	KB9022 +3VLP	+3VLP	+3VLP	X	X	+3VLP	X	X
EC_SMB_DA1	KB9022 +3VS	X	X	X	+3VS	X	X	+3VS
EC_SMB_DA2	CPU +3VALW	X	X	X	X	+3VS	X	X
SMBCLK	CPU +3VALW	X	X	X	X	X	X	X
SMBDATA	CPU +3VALW	X	X	X	X	X	X	X
SMLOCLK	CPU +3VS	X	X	X	X	X	X	X
SML0DATA	CPU +3VS	X	X	X	X	X	X	X
SML1CLK	CPU +3VS	X	X	X	X	X	X	X
SML1DATA	CPU +3VS	X	X	X	X	X	X	X

CPU part

U1 CPU1@ I7-4500U 1.8G C0 SA00006SLA0	U1 CPU2@ I3-4010U 1.7G C0 SA00006SX80	U1 CPU3@ I5-4200U 1.6G C0 SA00006SMC0	U1 CPU4@ I3-4100U 1.8G C0 SA00006SU30	U1 CPU5@ I3-4005U 1.7G D0 SA00007C200
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PCB part

ZZZ0 PCB 138 LA-A921P REV0 M/B 3 DA8000Z0000
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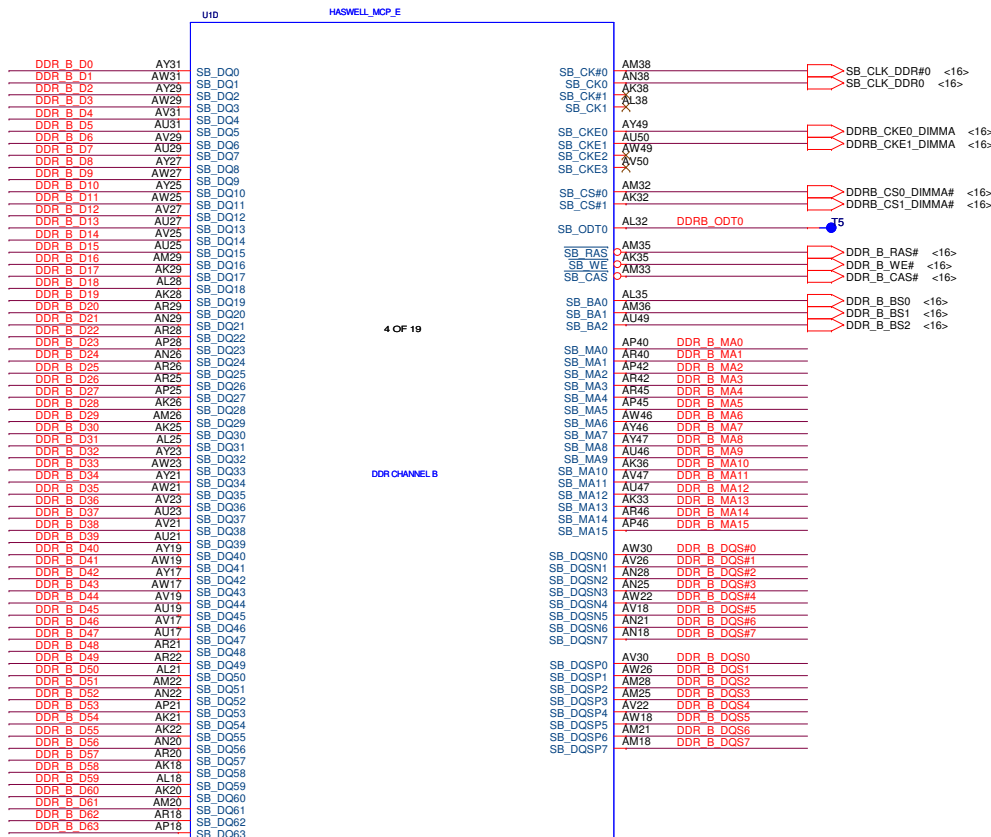
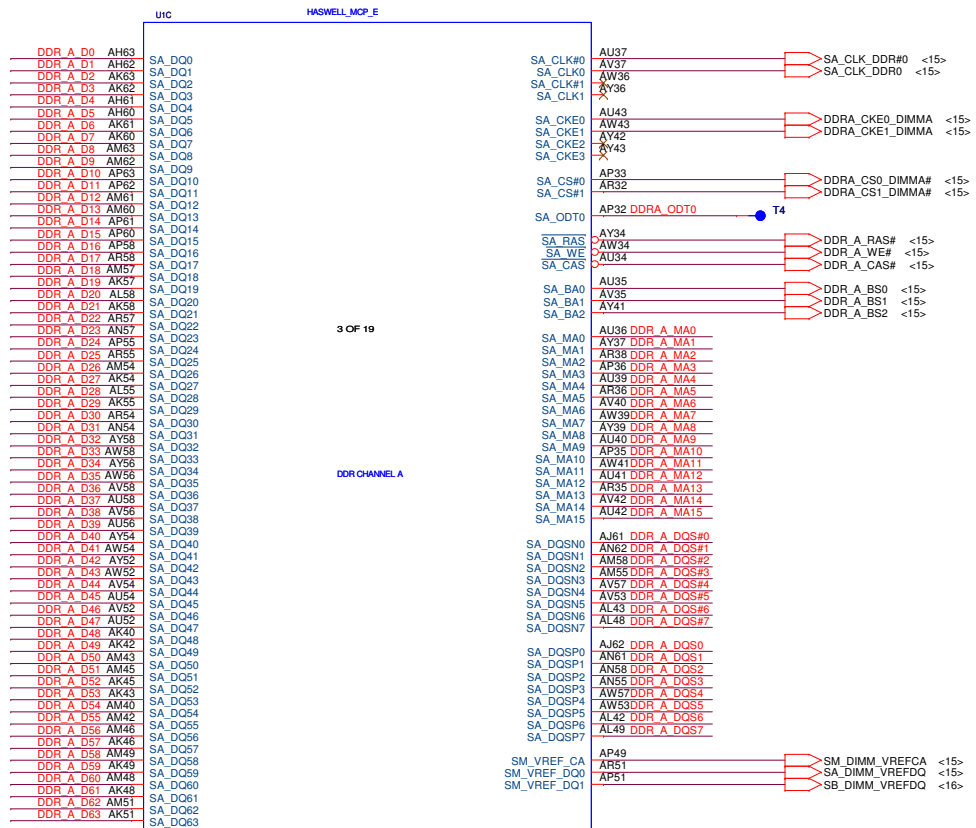
DRAM

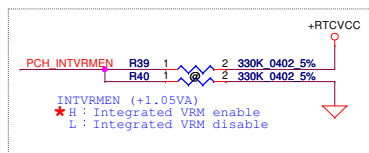
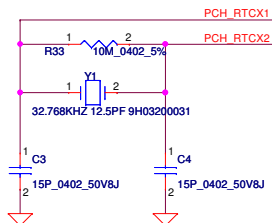
ZZZ3 H4G@ HYNIX X7652B3BL02 H5TC4G63AFR-PBA SA00000SAV20	ZZZ4 E4G@ ELPIDA X7652B3BL03 EDJ4216EFBG-GN-F SA00000SBT40	ZZZ7 S4G@ SAMSUNG X7652B3BL01 K4B401646Q-HYK0 SA00000JC40	ZZZ8 M4G@ MICRON X7652B3BL04 MT41K256M16HA-125:E SA00000SD010	ZZZ9 S8G@ SAMSUNG X7652B3BL05 K4B8G1646Q-HYK0 SA00000SD010	ZZZ10 E8G@ ELPIDA X7652B3BL07 EDJ8416E6MB-GN-F SA00000GAU00	ZZZ5 M8G@ MICRON X7652B3BL06 MT41K512M16TNA-125E SA00000GAU00	ZZZ6 H8G@ HYNIX X7652B3BL06 H5TC8G63AMR-PBA SA00000SK200
--	--	---	---	--	---	---	--

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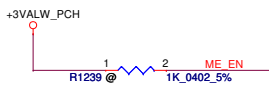
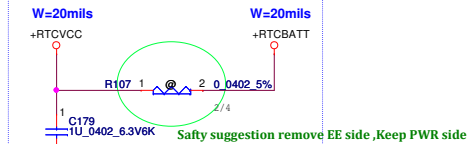
<15> DDR_A_D[0..63]
<15> DDR_A_MA[0..15]
<15> DDR_A_DQS#[0..7]
<15> DDR_A_DQS[0..7]

<16> DDR_B_D[0..63]
<16> DDR_B_MA[0..15]
<16> DDR_B_DQS#[0..7]
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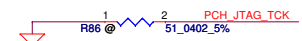




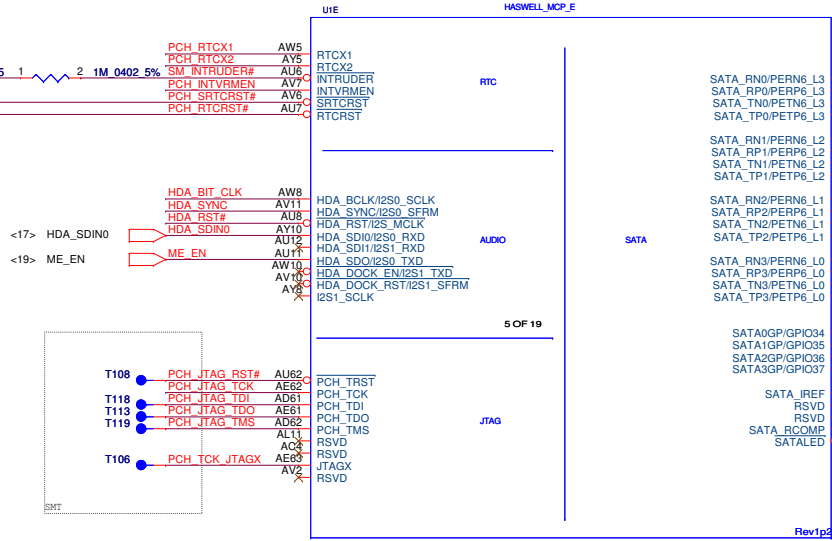
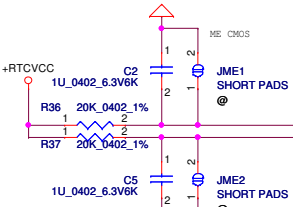
RTC Battery



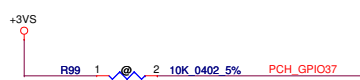
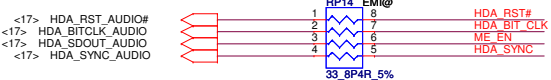
ME_EN
 ME debug mode, this signal has a weak internal PD
 * Low = Disabled (Default)
 High = Enabled [Flash Descriptor Security Override]



JME2 Short PAD placement to Bottom side.

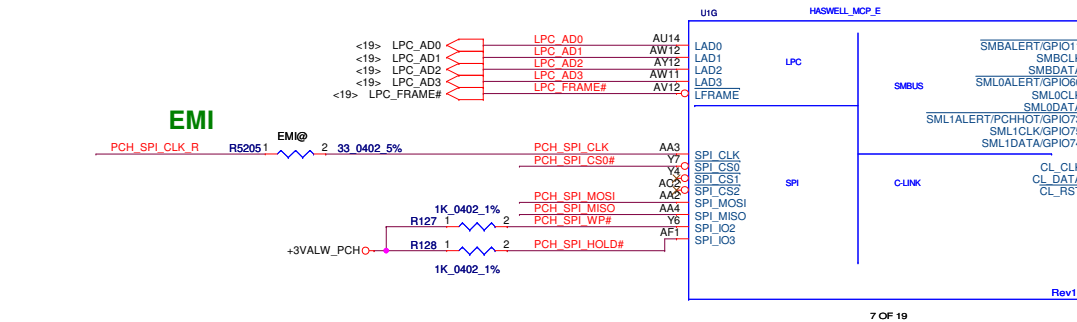
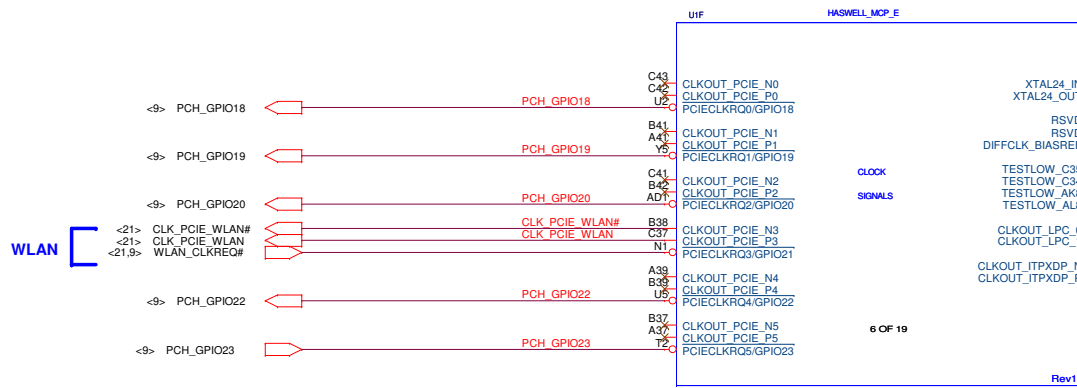


EMI

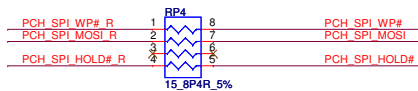


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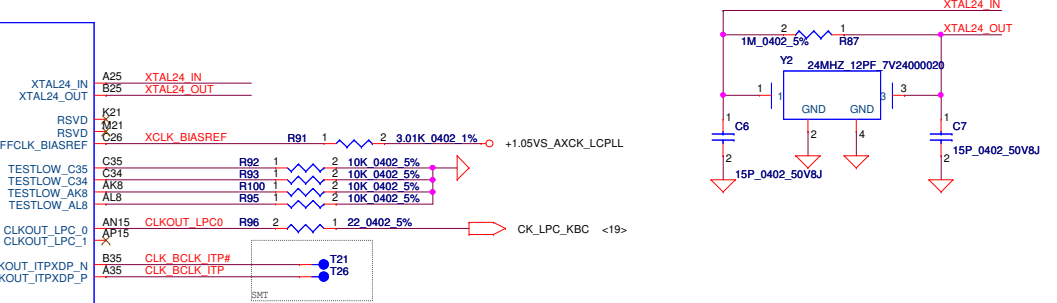
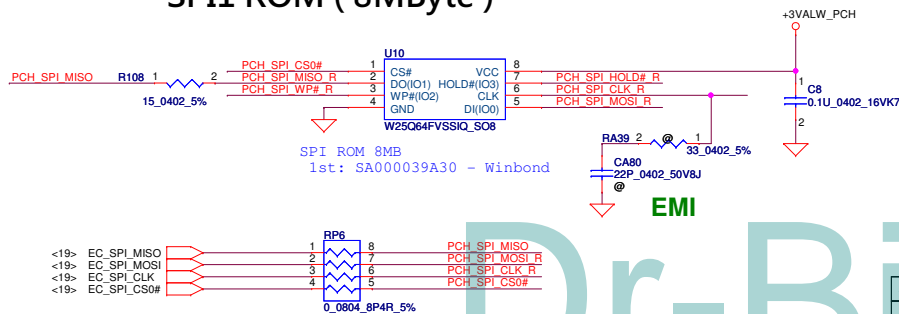
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CHKLIST1.0
2 SPI Device = 33 ohm
1 SPI Device = 15 ohm

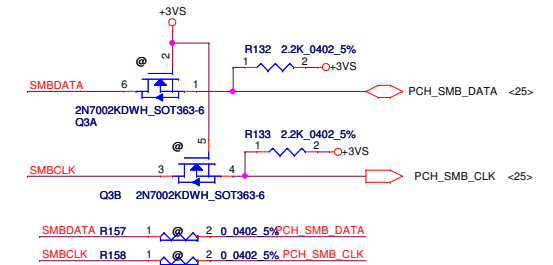


SPI1 ROM (8MByte)



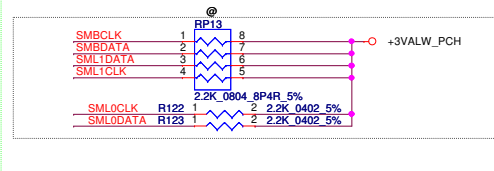
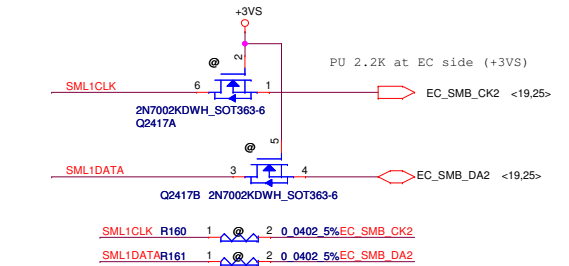
SMBus :TP

FootPrint :DMN66D0LDW-7_SOT363-6

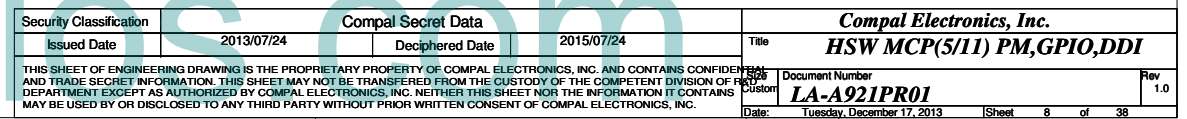


SML1 Bus :EC/Thermal Sensor

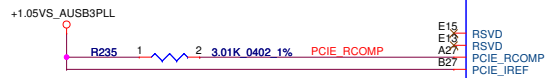
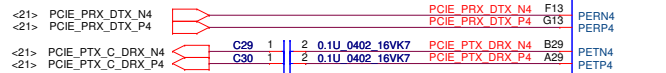
FootPrint :DMN66D0LDW-7_SOT363-6



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WLAN

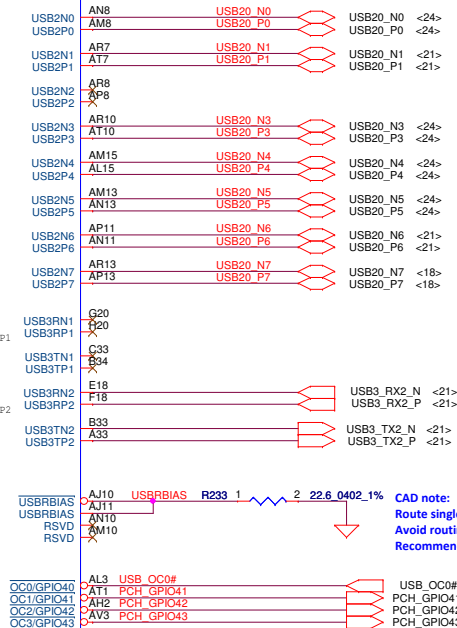


U1K HASWELL_MCP_E

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PCIE

USB

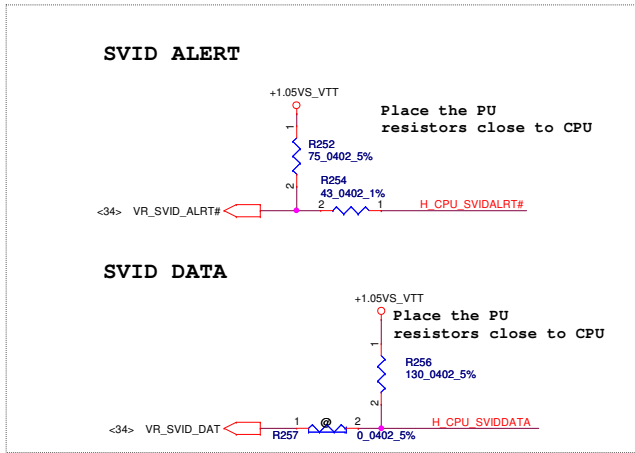
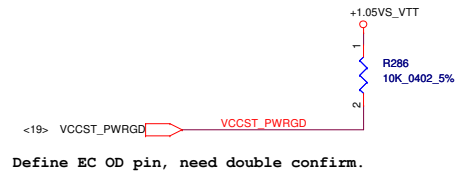


USB2 IO (Sub Board)
USB2/3 IO (Main Board)
Card Reader
Touch Screen
Camera
Mini Card(WLAN+BT)
Sensor

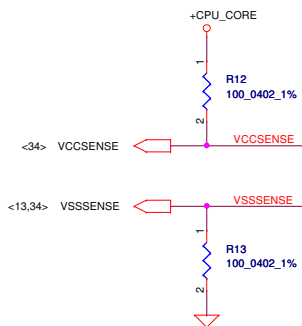
USB2/3 (Main Board)

CAD note:
Route single-end 50-ohms and max 450-mils length.
Avoid routing next to clock pins or under stitching capacitors.
Recommended minimum spacing to other signal traces is 15 mils

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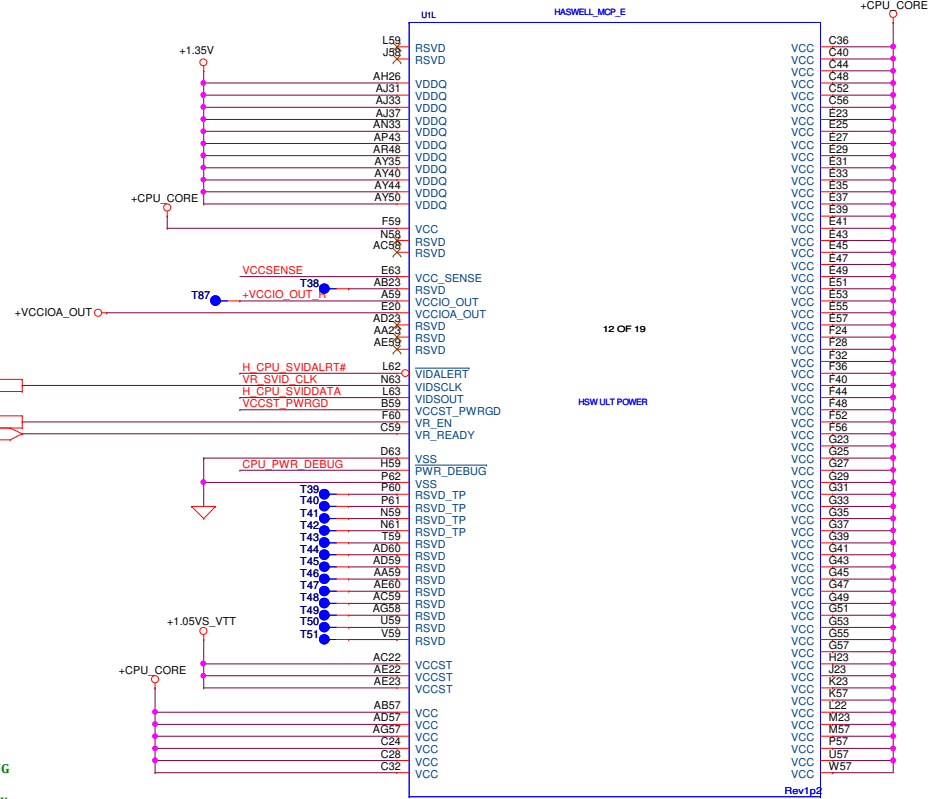
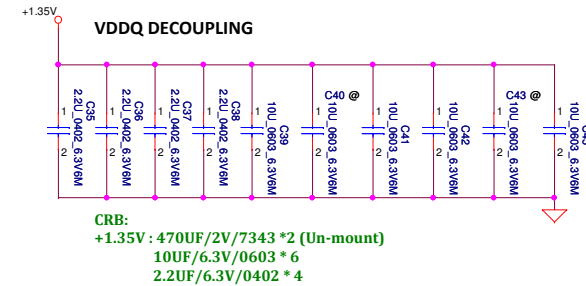
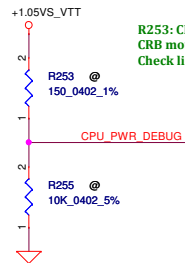
R256:
CRB r0.7 changed from 130 Ohms to
110 Ohms



CAD Note: PU resistor should be close to CPU

CAD Note: PD resistor should be close to CPU

R253: CPU_PWR_DEBUG
CRB mount
Check list_XDP use only



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[illegible]

+1.05VS_VTT

+3VALW_PCH ○ C78 1 | 2 22U 0603 6.3V6M ▷

+3VS ○ C82 1 | 2 22U_0603 6.3V6M ▷

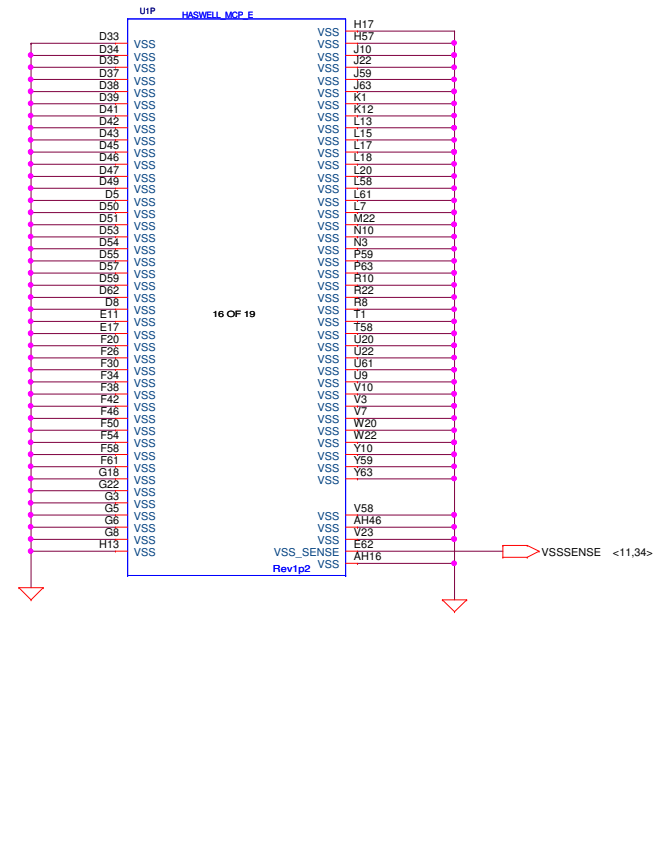
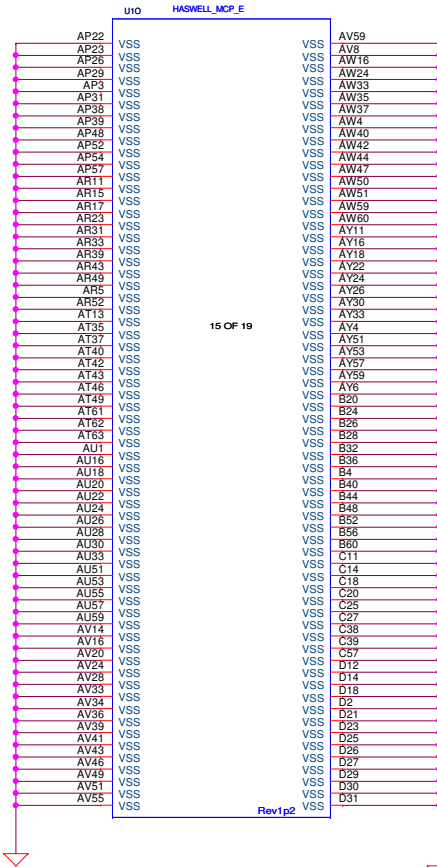
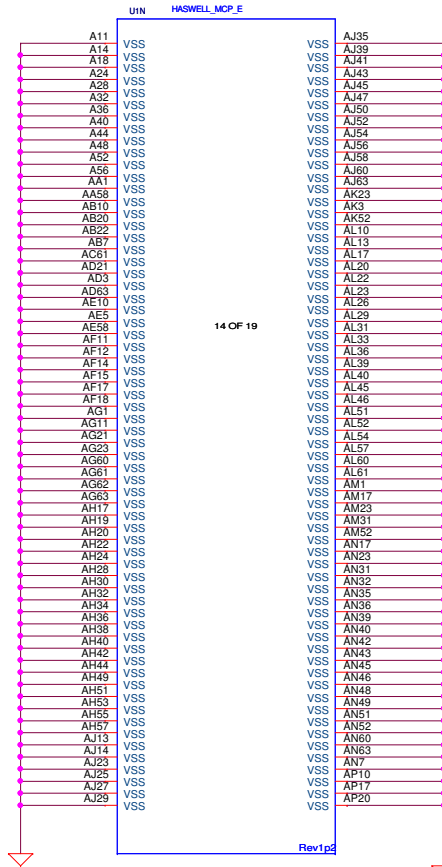
+1.05VS_VTT C87 1 2 1U 0402 6.3V6K

+1.05VS_VTT C88 1 2 1U_0402_6.3V6K

+3VALW PCH C75 2 | 1 1U_0402_6.3V6K

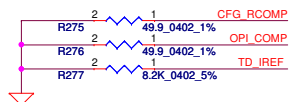
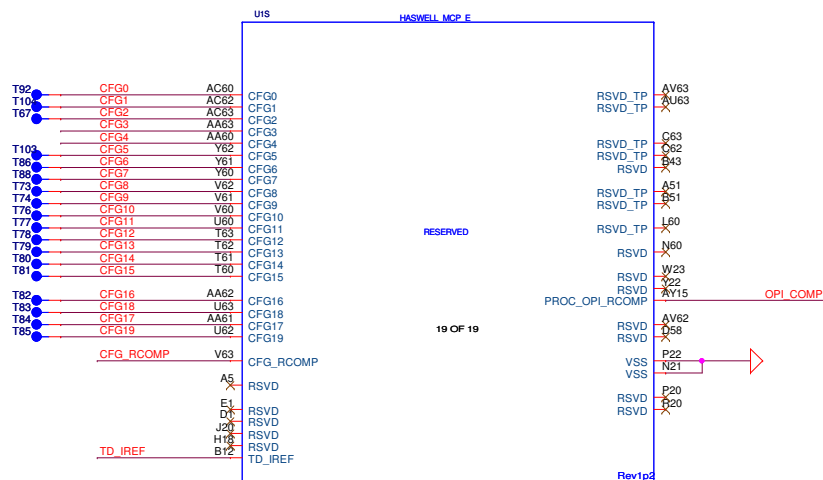
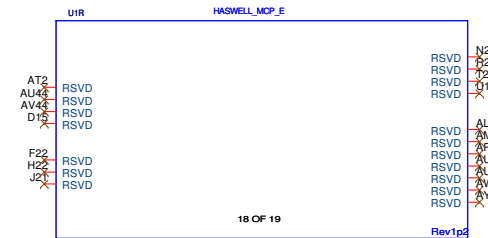
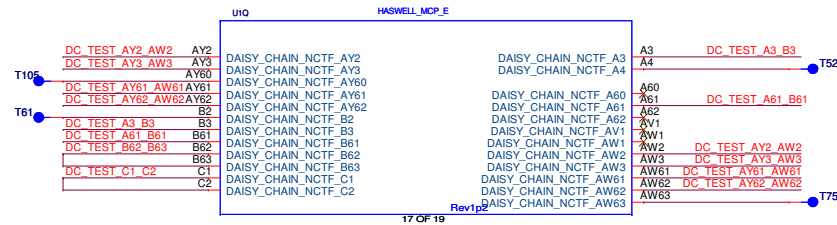


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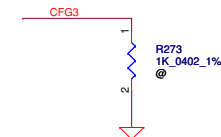


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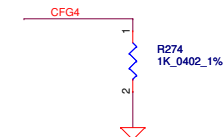
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CFG Straps for Processor



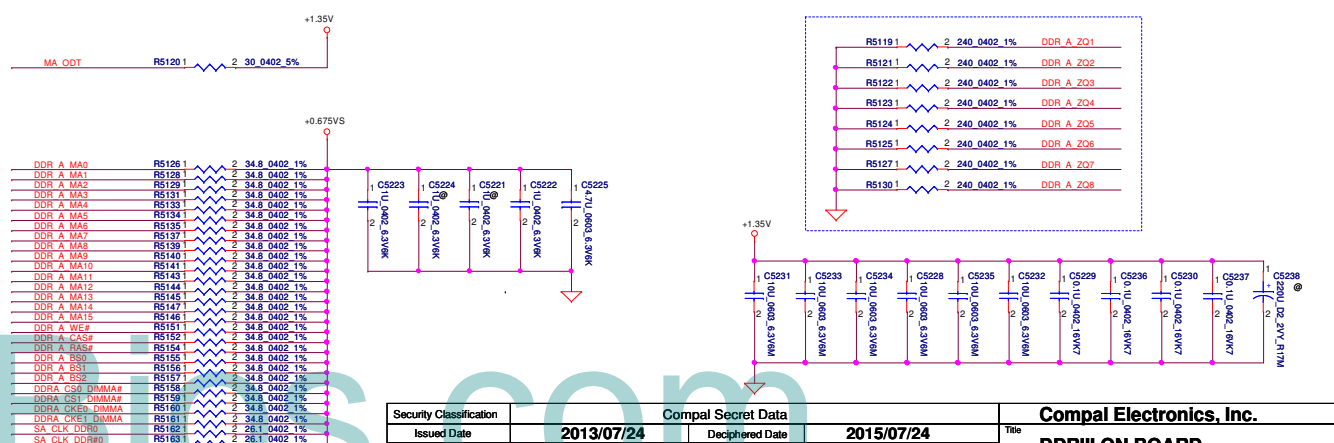
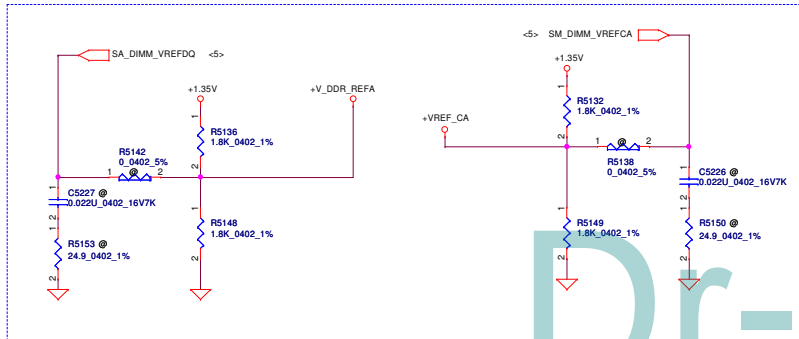
Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



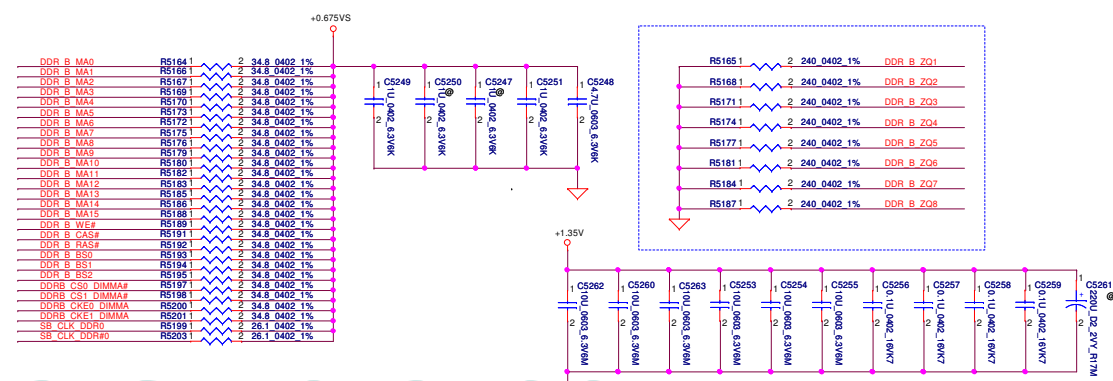
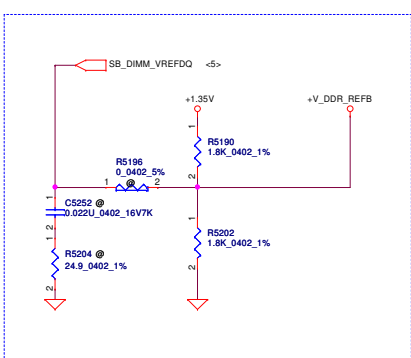
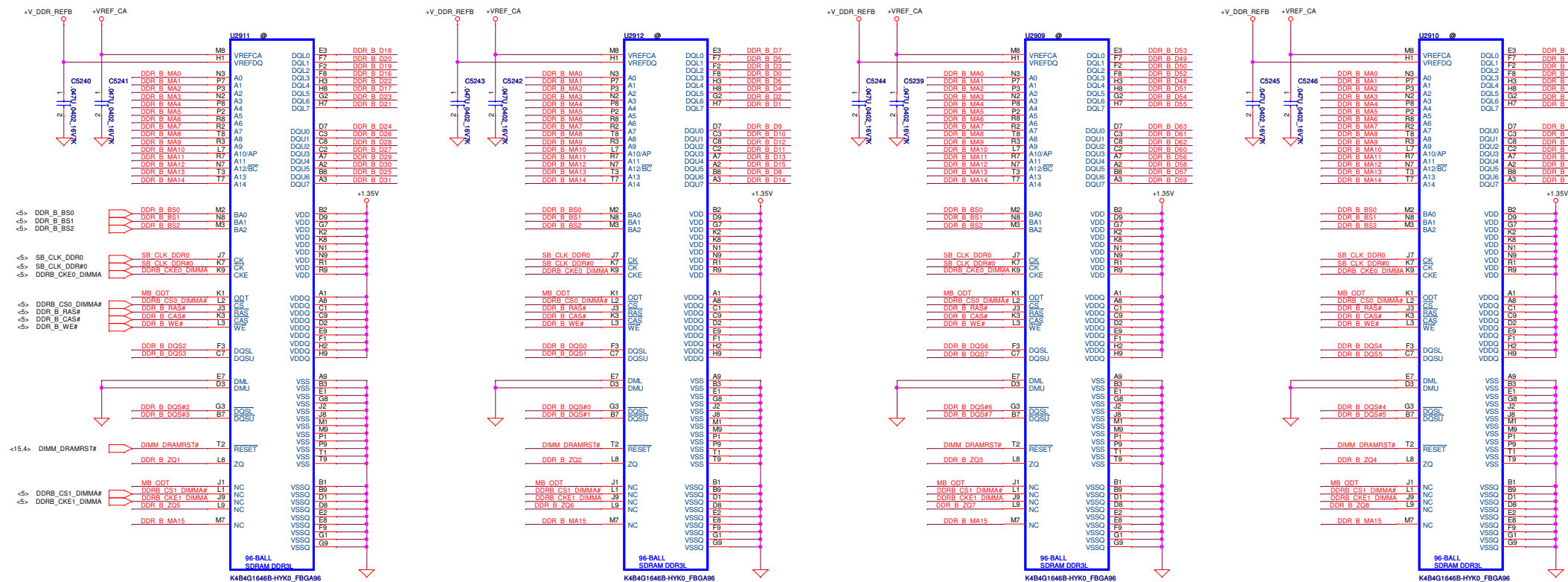
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

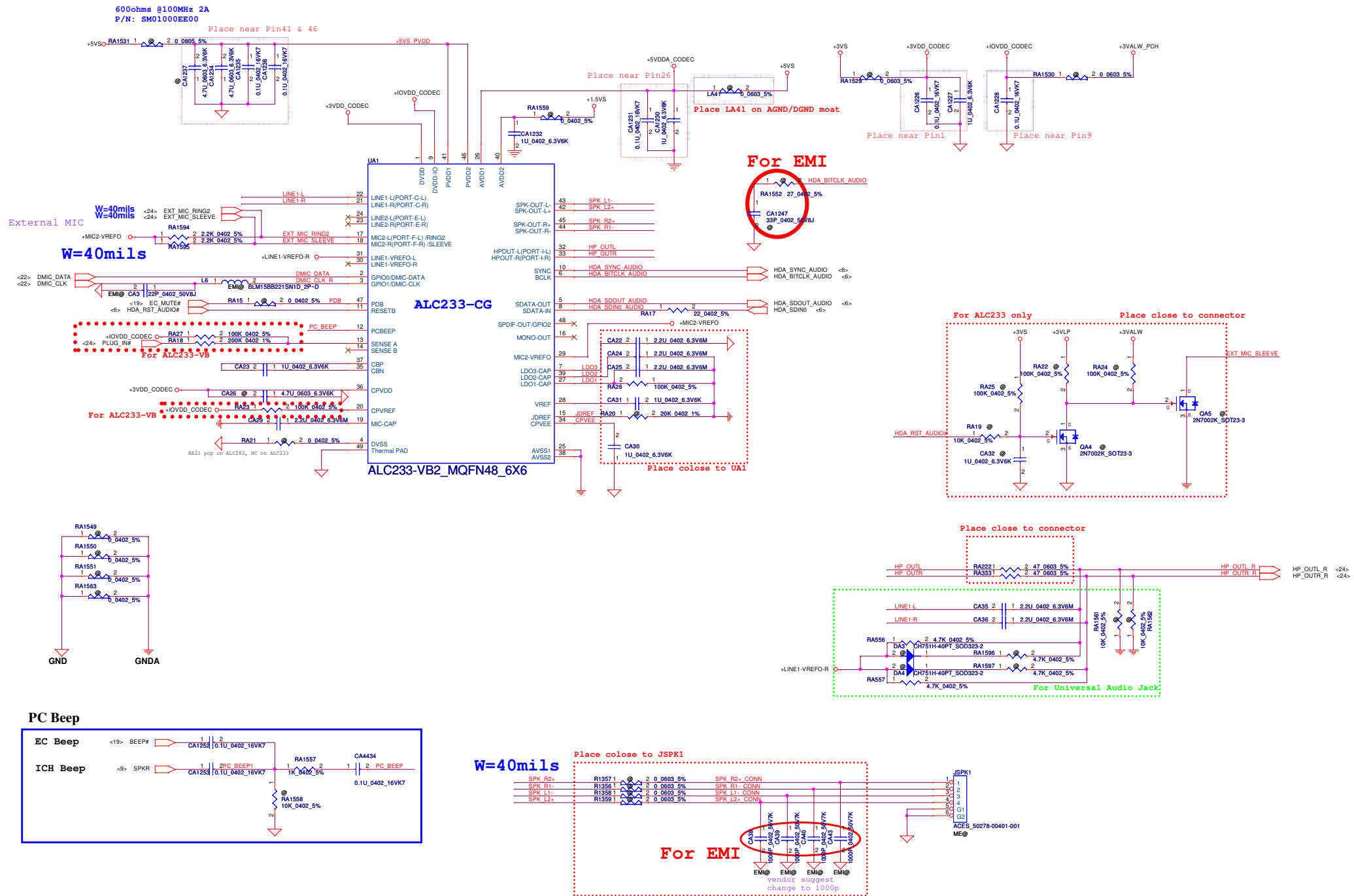
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Size	Custodian		Date	Rev
			14/07/2013	1.0

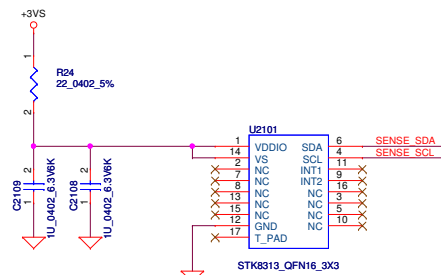




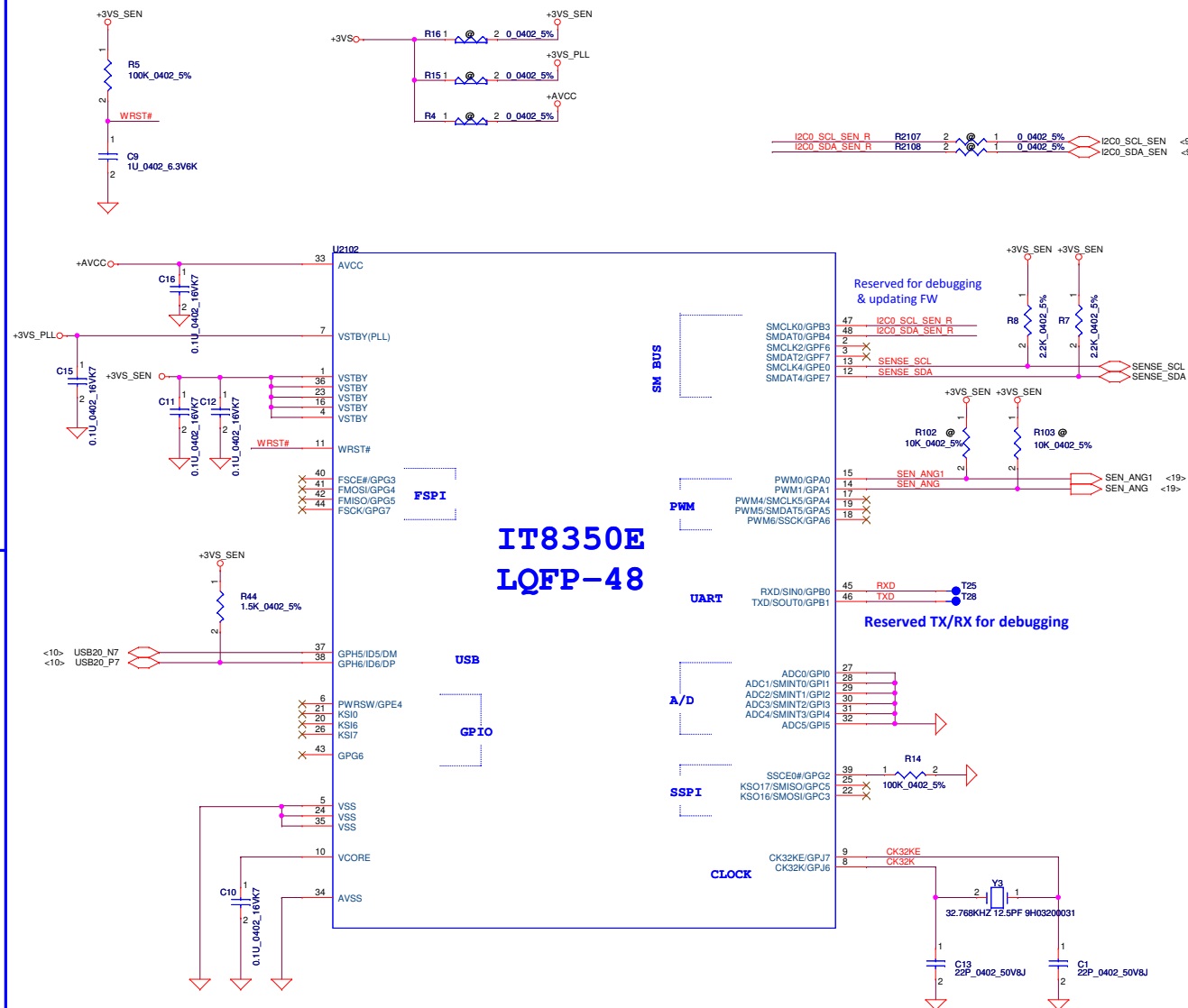
Dr-Bios.com

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Issued Date	2013/07/24	Deciphered Date	2015/07/24	Title	CODEC ALC233/Speaker CONN
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Size	Document Number	LA-A921PR01		Rev	1.0
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2nd G-sensor



Sensor Hub



IT8350E
LQFP-48

USB

GP:

SM BUS

PWM

UA

A/D

SSPI

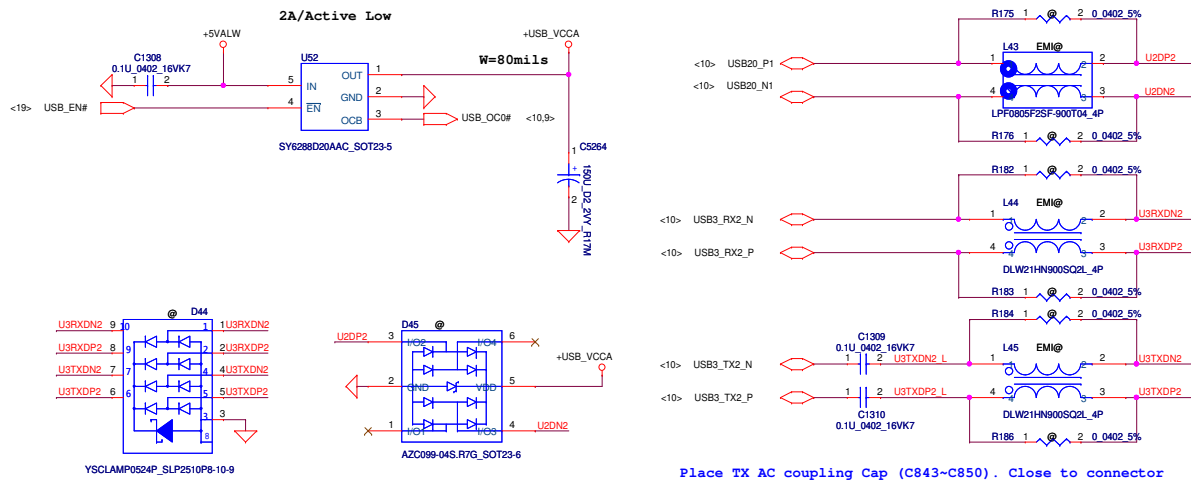
CLOCK

Reserved for debugging

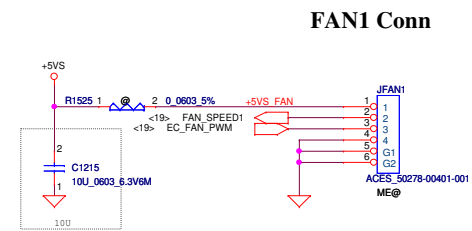
Reserved TX/RX for debugging

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Issued Date	2013/07/24	Deciphered Date	2015/07/24	Title	Sensor Fusion
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Date:		Tuesday, December 17, 2013		Sheet	18 of 38

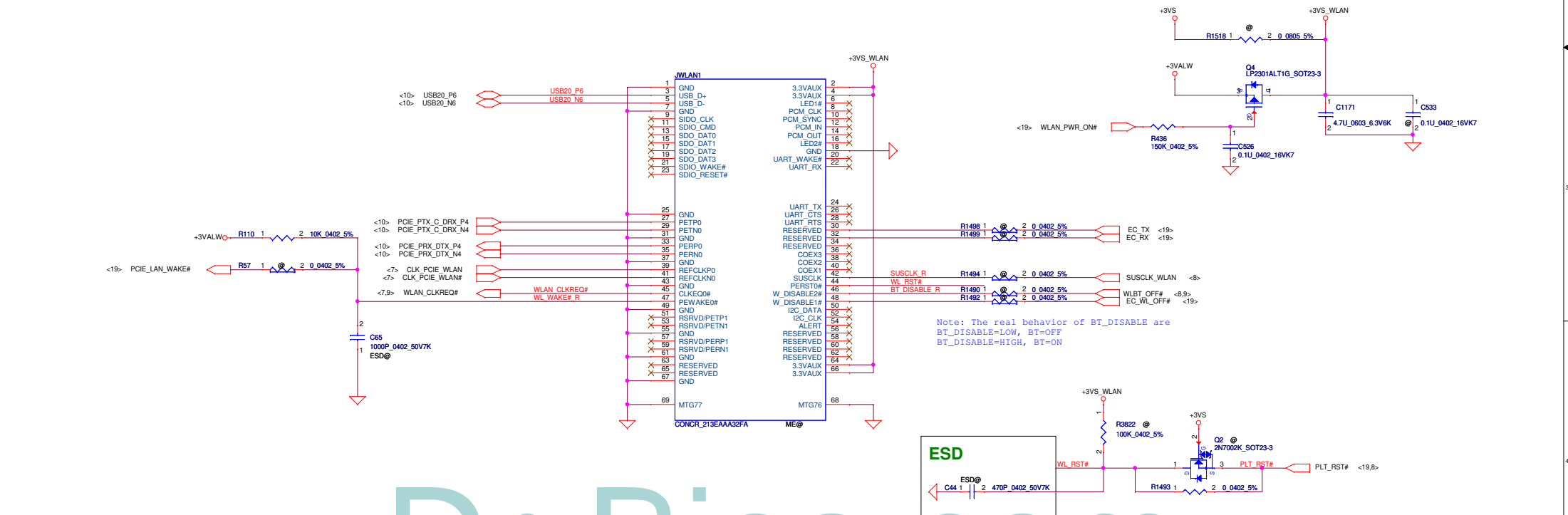
USB 3.0 Conn.



FAN CONN.

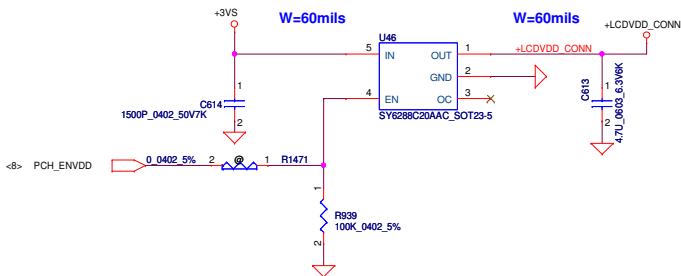


NGFF for WLAN(Key E)

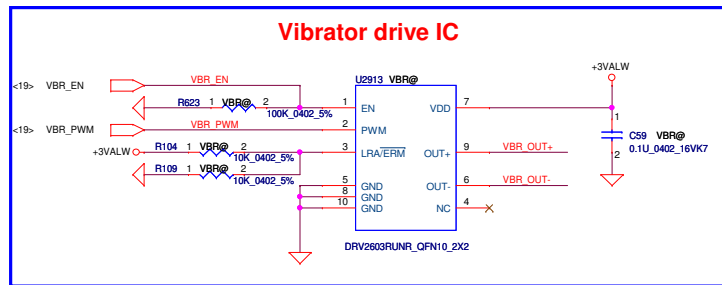


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Issued Date	2013/07/24	Deciphered Date	2015/07/24	Title	USB3.0/WLAN/FAN
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					Document Number
					LA-A921PR01
					Rev
					1.0
					Date: Tuesday, December 17, 2013
					Sheet 21 of 38

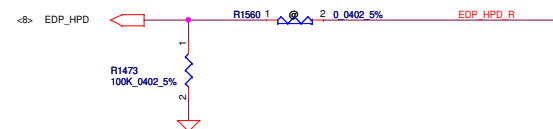
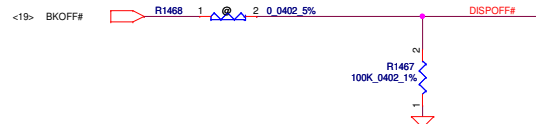
LCD POWER CIRCUIT



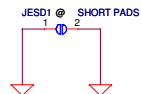
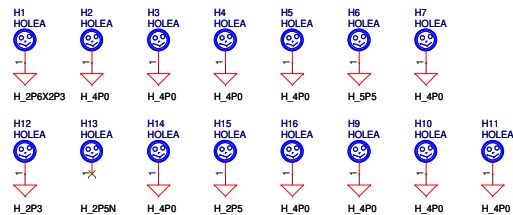
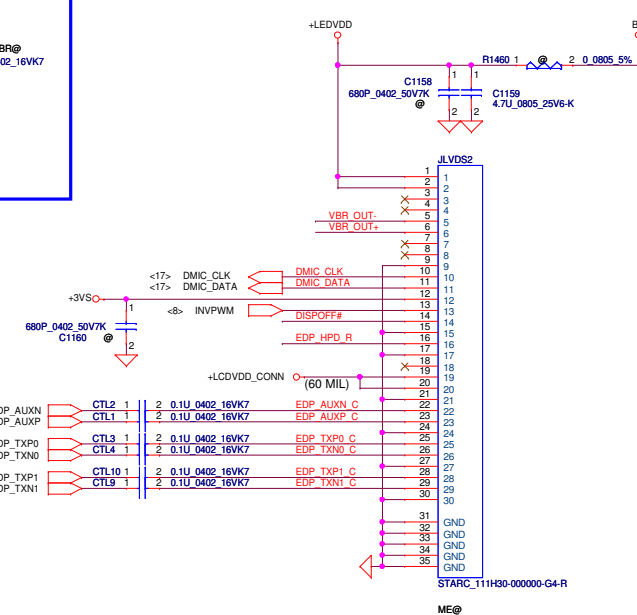
RTD2132R Internal load switch for +LCD_VCC



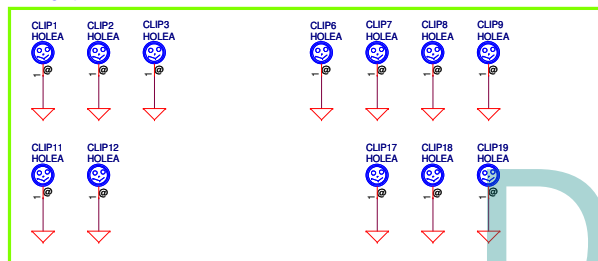
W=60mils



eDP PANEL BD. Conn.

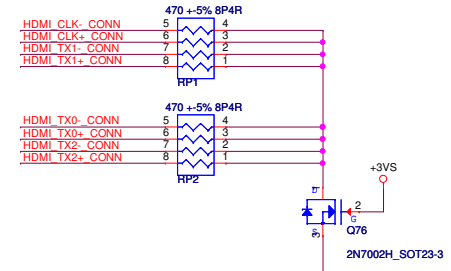
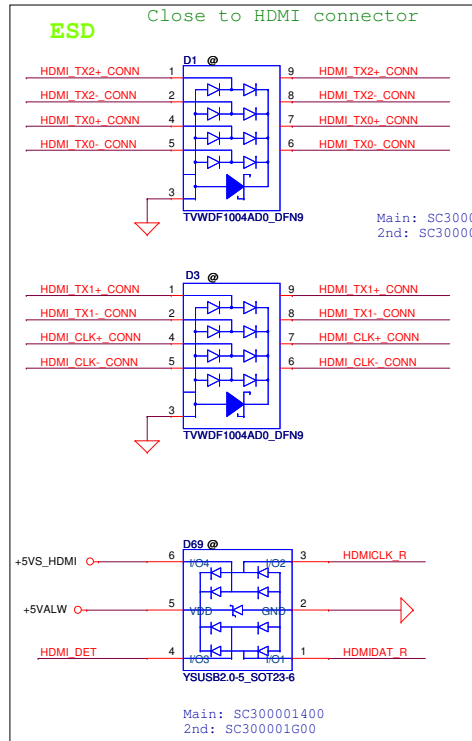
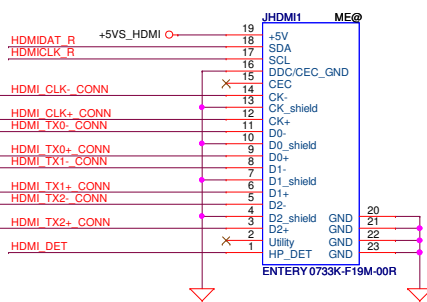
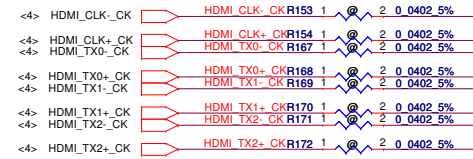
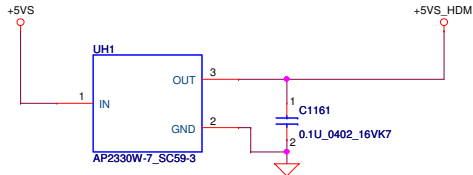
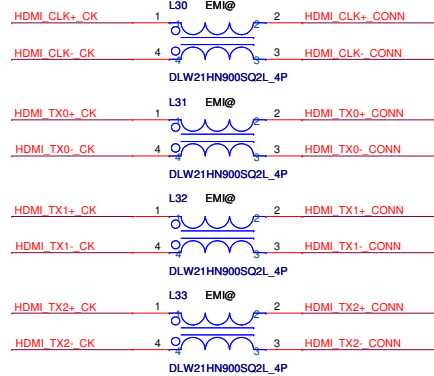
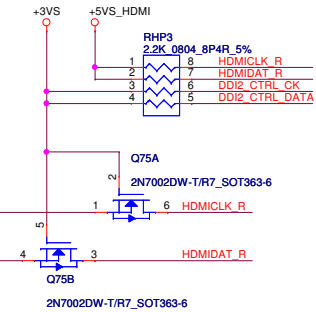


Shielding Clip



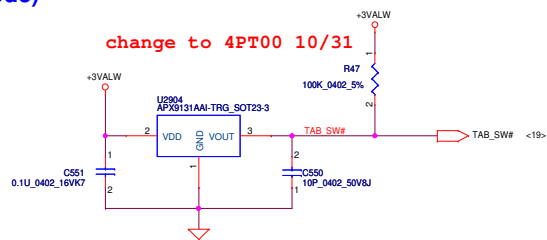
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Issued Date		Deciphered Date		eDP /DMIC/ HOLE	
2013/07/24		2015/07/24		LA-A921PR01	
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Sheet		22		of	
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<8> DD12_HDMI_HPD

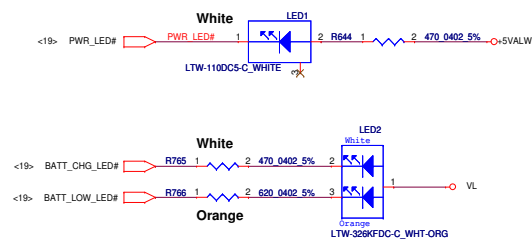


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				Date: Tuesday, December 17, 2013	Rev 1.0
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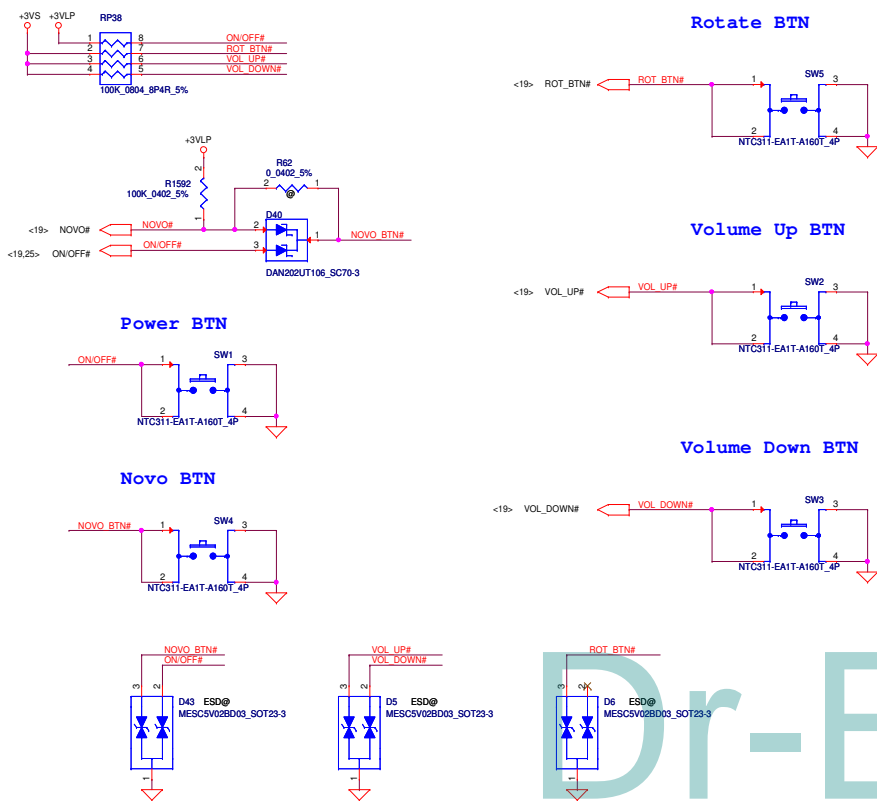
Lid SW(Tablet Mode)



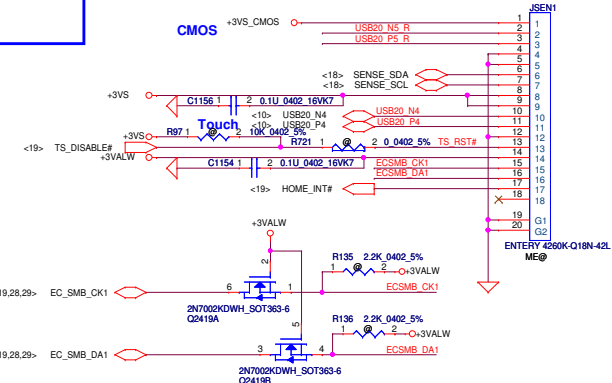
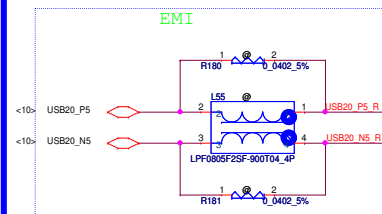
LED



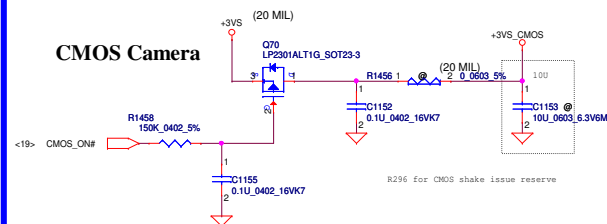
BUTTON



Touch & CMOS Conn

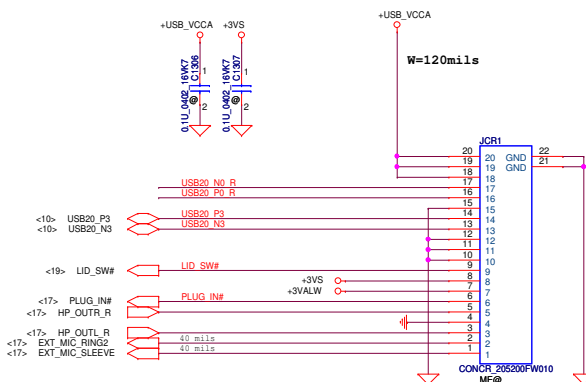
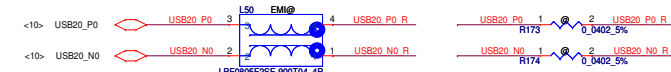


CMOS Camera



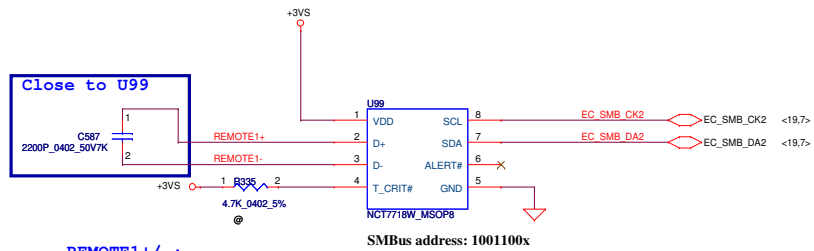
I/O Board

EMI

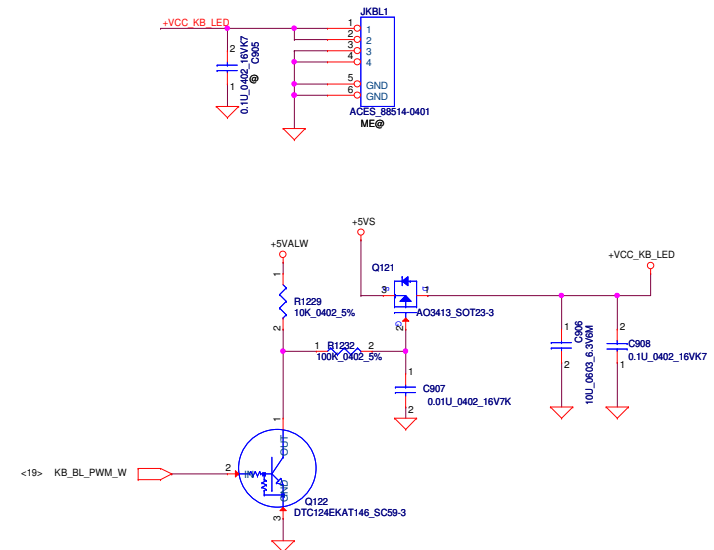


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Title		Compal Electronics, Inc.	
Size		Daughter board/LED/BTN/LID	
Date		Tuesday, December 17, 2013	
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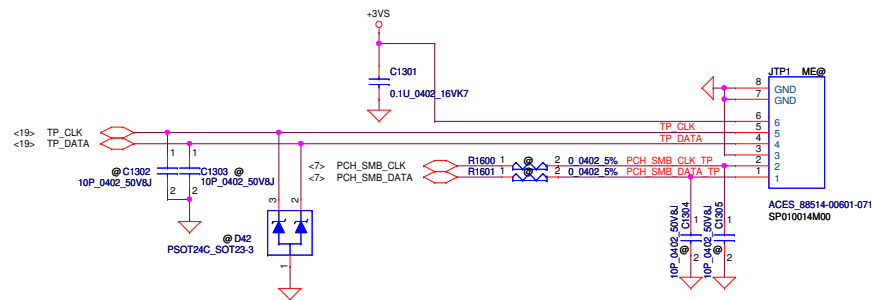
Thermal Sensor



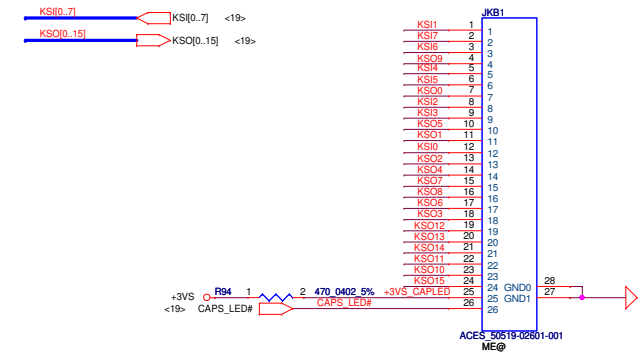
Keyboard Backlight



Click Pad

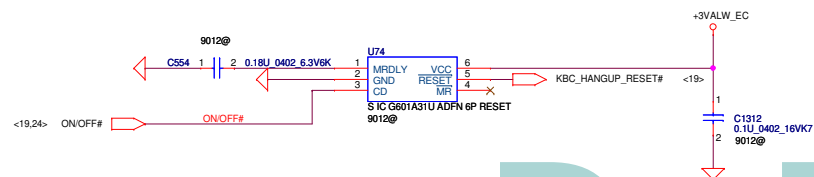


Keyboard



EC Reset IC

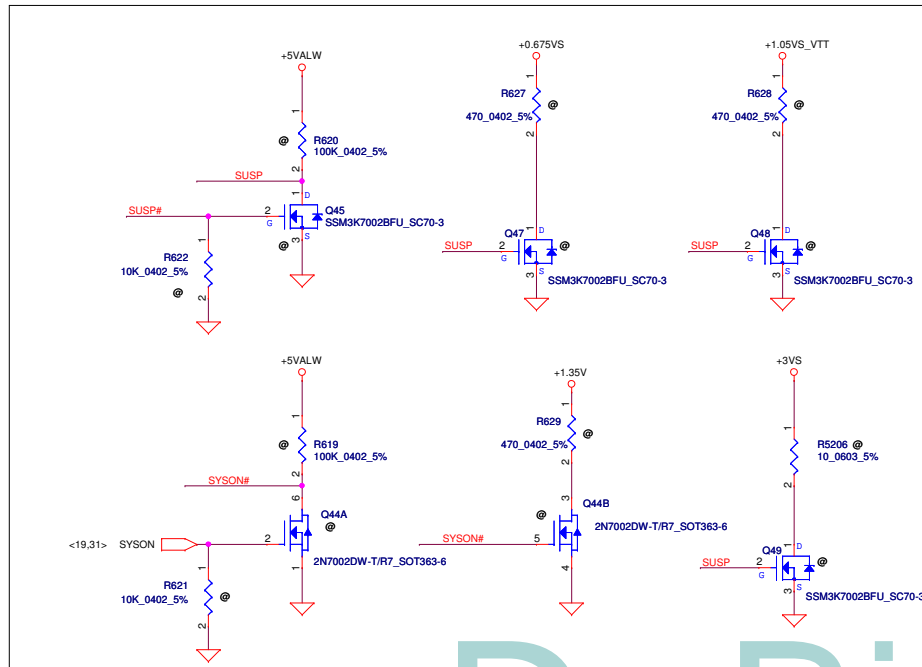
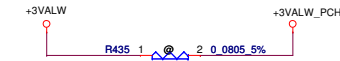
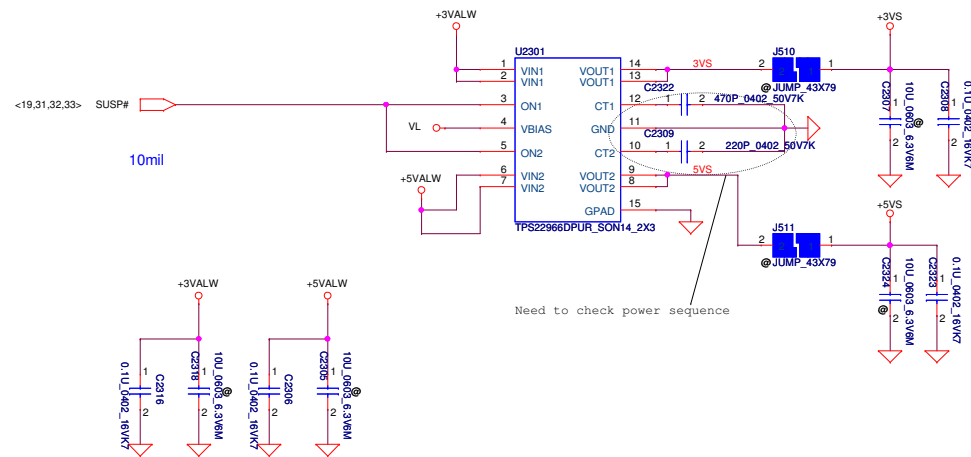
EC RESEST function



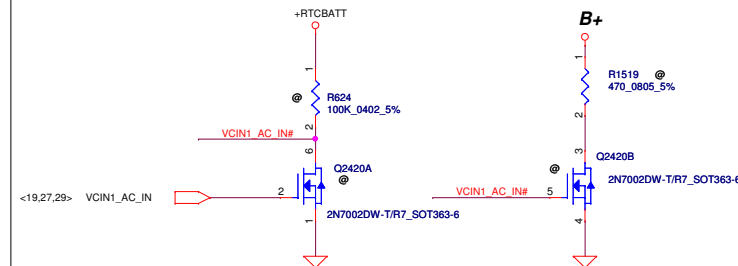
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Issued Date	2013/07/24	Deciphered Date	2015/07/24	Title	KB/TP/Thermal Sensor
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				Custom	LA-A921PR01
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+5VALW TO +5VS
+3VALW TO +3VS

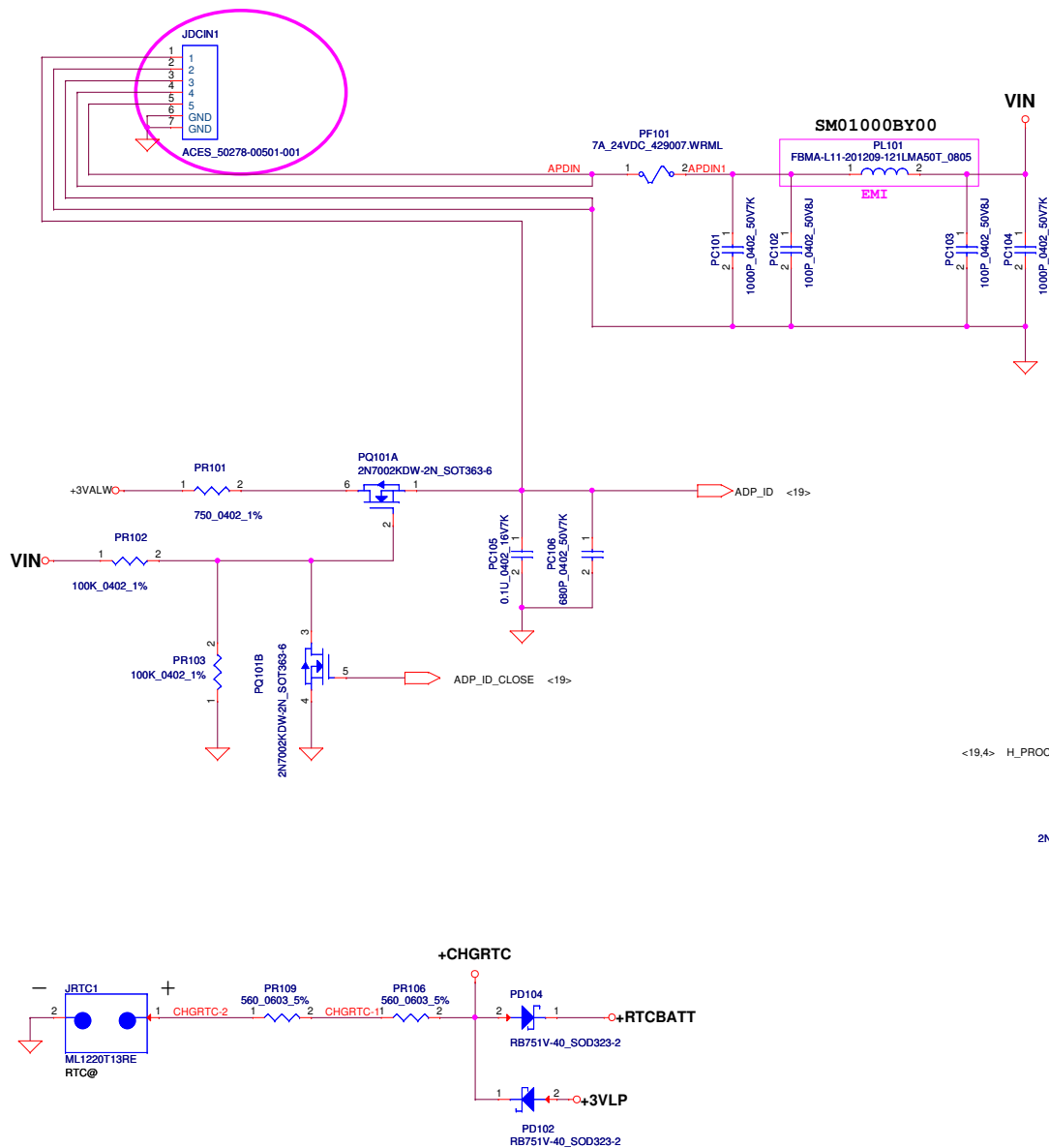
+3VALW TO +3VALW(PCH AUX Power)
+5VALW TO +5VALW(PCH AUX Power)



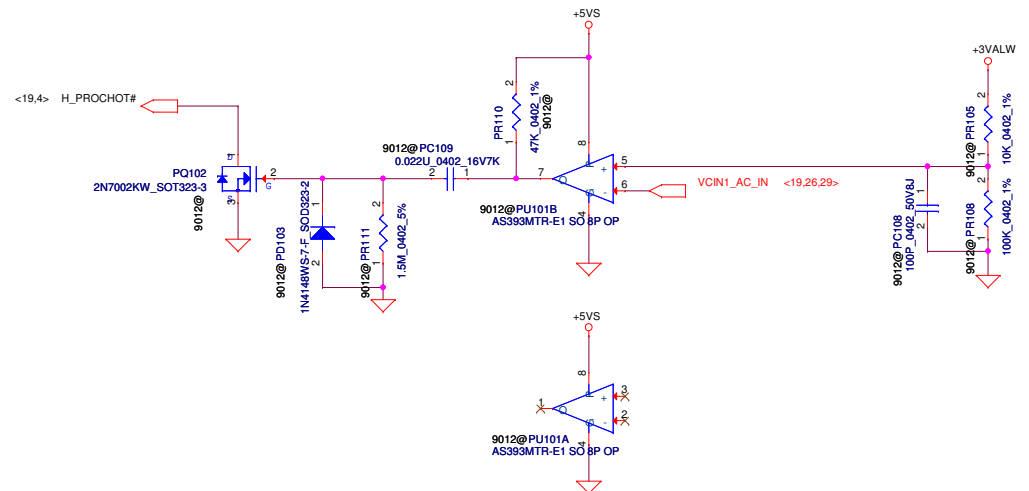
B+ dischager



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/07/24	Deciphered Date	2015/07/24	Title DC V TO VS INTERFACE		
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For KB9012 : Keep PU101 One-shot circuit
For KB9022 : Remove PU101 One-shot circuit



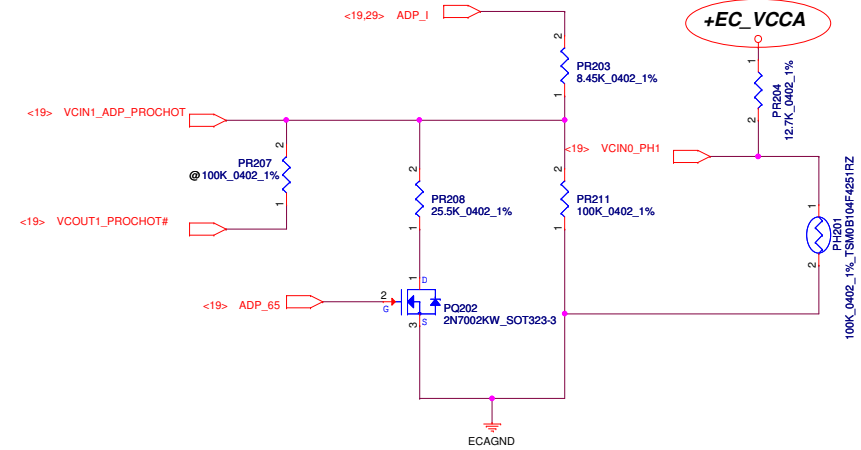
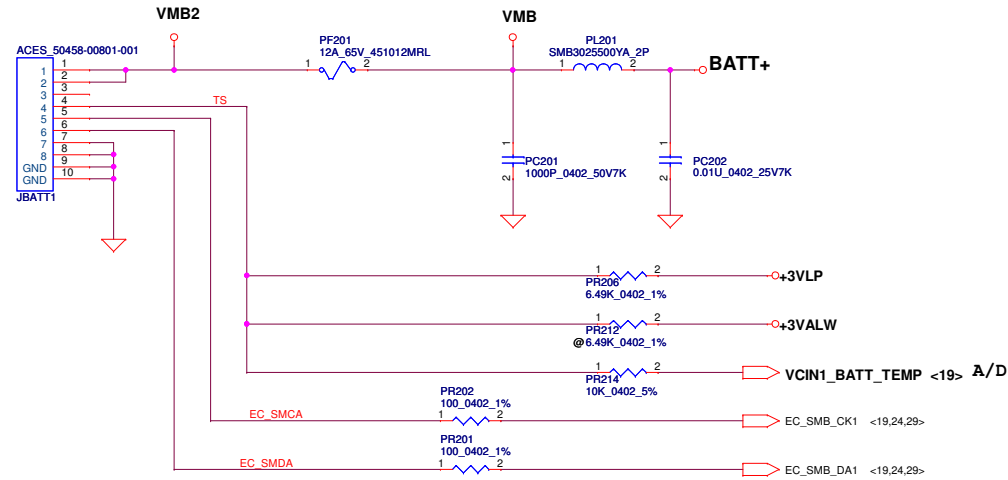
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2011/06/15	2012/07/11		
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Title		Date	
PWR DCIN / RTC Battery		Tuesday, December 17, 2013	
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PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

65W(UMA): 85W active W recovery

20120314
Change to +EC_VCCA from +3VLP

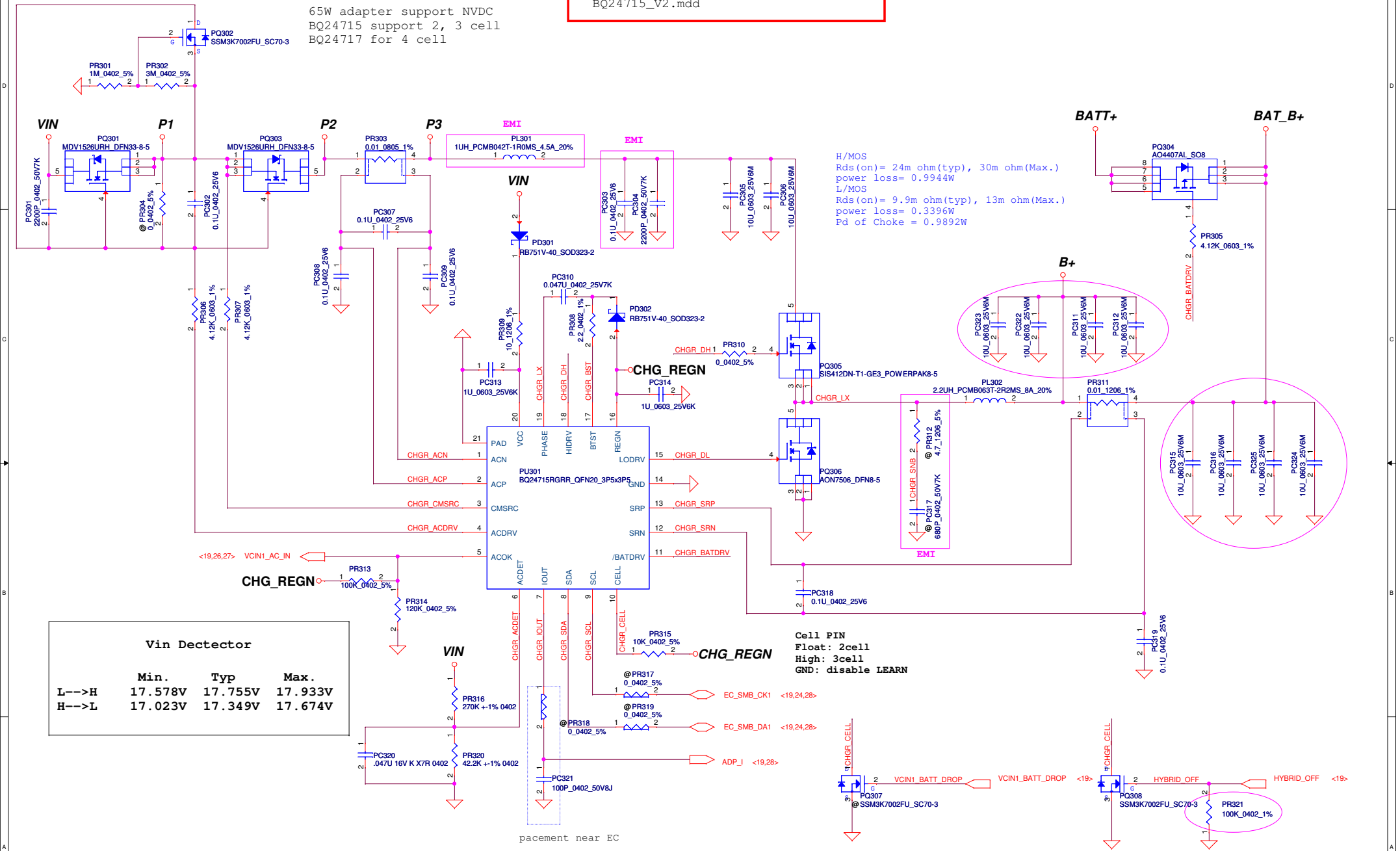


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BQ24715_V2.mdd

```
65W adapter support NVDC
BQ24715 support 2, 3 cell
BQ24717 for 4 cell
```



Vin Detector			
	Min.	Typ	Max.
L-->H	17.578V	17.755V	17.933V
H-->L	17.023V	17.349V	17.674V

placement near EC

Security Classification		Compal Secret Data				Compal Electronics, Inc.													
Issued Date		2012/04/03		Deciphered Date		2014/12/31		Title											
								CHARGER											
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										Size		Document Number						Rev 1.0	
										Date:		Tuesday, December 17, 2013				Sheet		29 of 38	

SY8208B_V2.mdd

ENLDO_3V5V



TDC=6A

TDC=6A



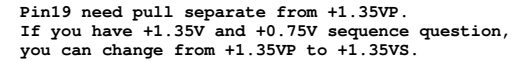
SY8208C_V2.mdd

5V LDO 150mA~300mA

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RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

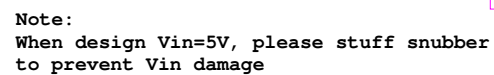


0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

Note: S3 - sleep ; S5 - power off

Switching Frequency: 285kHz
Ipeak=8A
Iocp~10A
OVP: 110%~120%
VFB=0.75V, Vout=1.354V
MOSFET footprint: SIS412DN

SY8003_V1.mdd

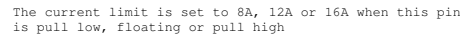


$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

$$V_{out} = 1.5V$$

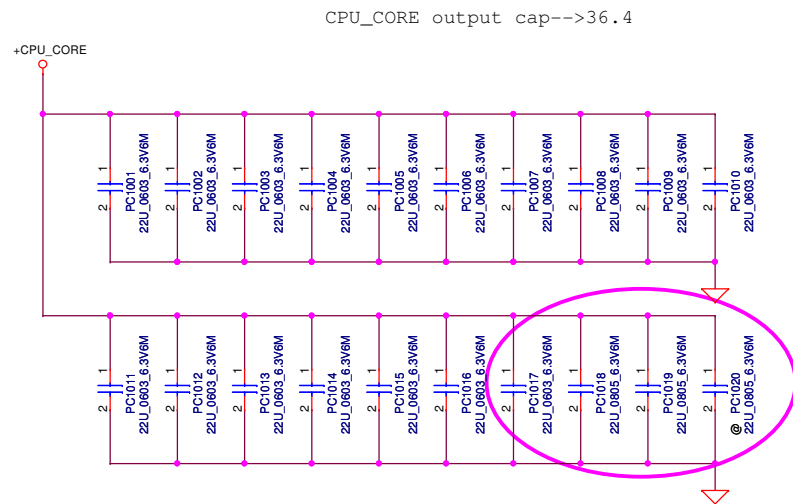
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Size Custom		Document Number				
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SY8208D_V1.mdd



Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

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				Document Number	1.0
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30 X 22uF 0805
2012/10/23
check the output cap Qty!!!
2012/10/24
23 pcs 22uF and reserve 7 pcs
2013/01/14
22uF*15; reserve 22uF*5

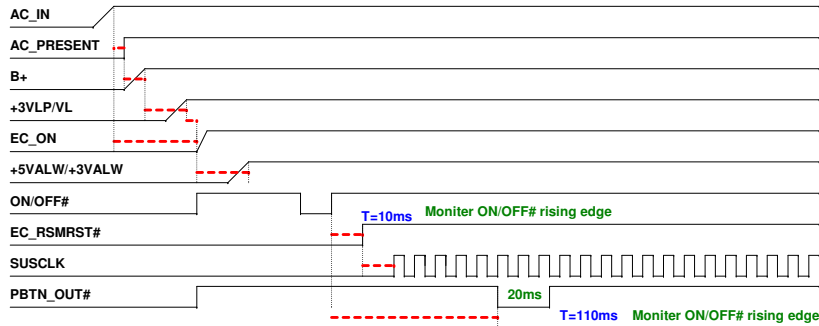
2013/09/6 22U_0603x17 + 22U_0805x2

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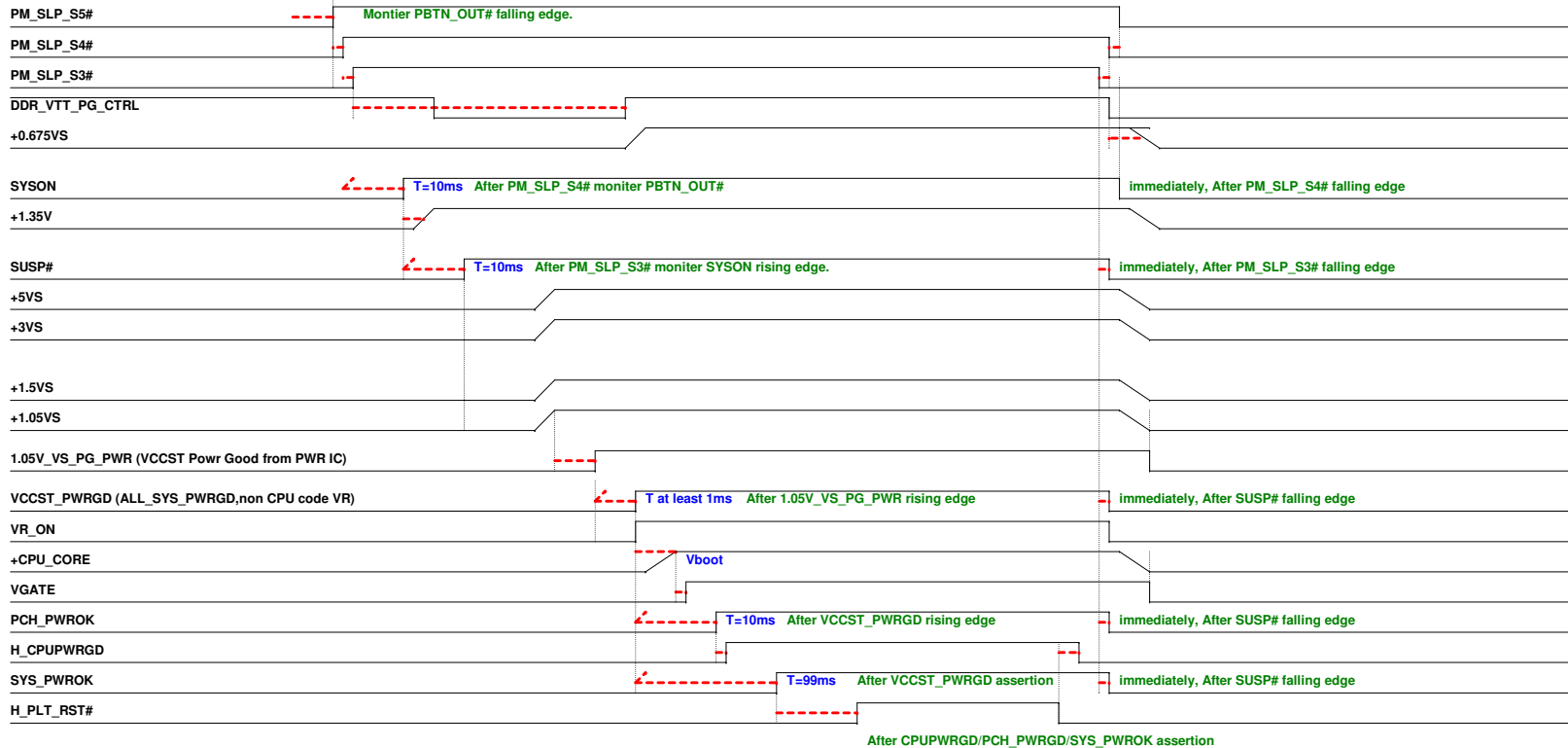
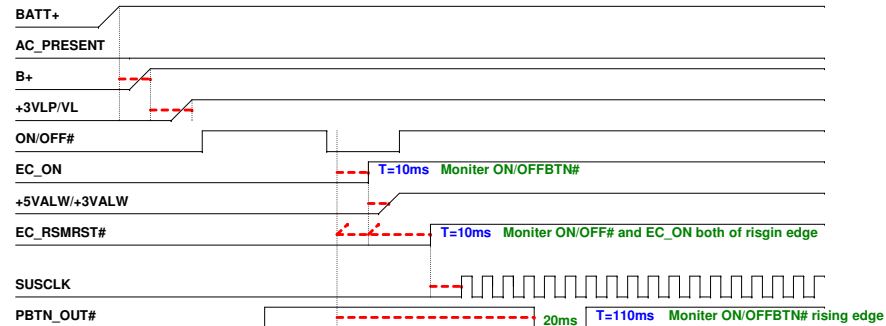
Item	Reason for change	PG#	Modify List	Phase
1	For ME design change	21,23	JHDMI1,JUSB1 change connector type	EVT
2	For ME design change	24	SW1,SW2,SW3,SW4,SW5 change type	EVT
3	For ME design change	24,25	JCR1,JKB1 change connector type	EVT
4	For EC pin common design	19	EC pin 25,27,38,86,123 control pin change	EVT
5	Follow EC power plane for EC_Reset	25	Change U74 power plan	EVT
6	For DVT phase MB ID	19	R1564 change from 43K to 27K	EVT
7	For BDW HDMI request	23	RP1,RP2 change value from 680ohm to 470ohm	EVT
8	For Audio vender recommend	17	1. Un-mount RA19,RA22 2. Mount RA1551,RA1563 3. Add CA1,CA2	EVT
9	For EMI request	17	R55 change to Bead	EVT
10	For Compal component policy	9,21	U52,U4 change type	EVT
11	For touch vennder recommend	24	1. JSEN1 pin 13 add 10K pull high 2. JSEN1 pin 14 change to +3VALW	EVT
12	For SPEC change	6,20	Delete SSD PCIE interface component	EVT
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